AMENDMENTS TO THE SPECIFICATION

After the paragraph ending on page 10, line 2, of the substitute specification filed with the Preliminary Amendment, please reinsert the following twenty-two paragraphs.

In the pulse generator circuit according to the invention, an additional clock pulse field effect transistor can be provided, at the gate terminal of which the clock signal can be applied, at the first source/drain terminal of which a second electrical reference potential can be applied, and the second source/drain terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor.

Furthermore, an additional feedback field effect transistor can be provided, the gate terminal of which is coupled to the gate terminal of the feedback field effect transistor, at the first source/drain terminal of which the second electrical reference potential can be applied, and the second source/drain terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor.

In addition, the pulse generator circuit can have a bypass field effect transistor, the gate terminal of which is coupled to the flip flop circuit, at the first source/drain terminal of which the first electrical reference potential can be applied, and the second source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor.

As an alternative, the pulse generator circuit can have a bypass field effect transistor, the gate terminal of which is coupled to the flip flop circuit, the first source/drain terminal of which is coupled to the first source/drain terminal of the feedback field effect transistor, and the second source/drain terminal of which is coupled to the second source/drain terminal of the clock pulse field effect transistor.

According to the embodiment described last, none of the source/drain terminals of the bypass transistor are connected to an electrical reference potential (for example an electrical ground potential) but are coupled to the source/drain terminals of the feedback field effect transistor or of the clock pulse field effect transistor, respectively. This improves the functionality of the pulse generator circuit since in the branch switched off, the so-called stack effect is active as a result of which the leakage current is reduced on this path.

The first electrical reference potential can be an electrical ground potential and/or the second electrical reference potential can be an electrical supply potential.

The clock pulse field effect transistor, the logic field effect transistor and the feedback field effect transistor can be field effect transistors of the n type of conduction.

The additional clock pulse field effect transistor and the additional feedback field effect transistor can be field effect transistors of the p-type of conduction.

The bypass field effect transistor can be a field effect transistor of the n-type of conduction.

Furthermore, a second signal path of additional field effect transistors which has the same circuit as the first signal path formed from the field effect transistors, is preferably provided in the pulse generator circuit, which additional field effect transistors are interconnected for generating from the clock signal and from a complementary data signal which is complementary to the data signal a complementary input signal which is complementary to the input signal of the flip flop circuit. According to this embodiment, the pulse generator circuit is constructed as a differential pulse generator circuit in which, to illustrate, a signal is provided which is in each case complementary to each signal.

In the second signal path, an identical or mirror-identical transistor is provided and interconnected for each transistor of the first signal path, to illustrate, particularly an additional clock pulse field effect transistor corresponding to the clock pulse field effect transistor, an

additional logic field effect transistor corresponding to the logic field effect transistor and an additional feedback field effect transistor corresponding to the feedback field effect transistor etc.

The first source/drain terminal of the additional clock pulse field effect transistor of the second signal path can preferably be coupled to the gate terminal of the additional feedback field effect transistor of the first data path.

The first source/drain terminal of the clock pulse field effect transistor of the first signal path can be coupled to the gate terminal of the additional feedback field effect transistor of the second data path.

Furthermore, the control unit 250 can be set up in such a manner that it applies the data signal to the gate terminal of the logic field effect transistor before the clock signal is switched for changing the clock pulse field effect transistor from a state with electrically nonconducting channel region into a state with electrically conducting channel region. According to this embodiment, a particularly advantageous order of applying the signal to the transistors of the cascade of feedback field effect transistor/logic field effect transistor/clock pulse field effect transistor is created, and thus a particularly fast signal processing for generating an input signal for the switching part-circuit or the flip flop part-circuit, respectively.

In the further text, the circuit arrangement according to the invention which has a pulse generator circuit according to the invention is described in greater detail. Embodiments of the pulse generator circuit also apply to the circuit arrangement having a pulse generator circuit.

The flip flop circuit of the circuit arrangement can have storage field effect transistors for storing storage signals based on the input signal and/or the complementary input signal. Of these storage field effect transistors, two field effect transistors of different type of conduction in each case can be interconnected in each case to form an inverter, so that the flip flop circuit is essentially formed from two inverters.

The flip flop circuit can have field effect transistors which are connected between the storage field effect transistors and the pulse generator circuit.

In particular, a first switching field effect transistor can be provided, the gate terminal of which is coupled to the first source/drain terminal of the clock pulse field effect transistor, at the first source/drain terminal of which the second electrical reference potential can be applied, and the second source/drain terminal of which is coupled to a storage node of the storage field effect transistors.

In addition, a second switching field effect transistor can be provided, the gate terminal of which is coupled to the gate terminal of the complementary bypass field effect transistor, at the first source/drain terminal of which the first electrical reference potential can be applied, and the second source/drain terminal of which is coupled to the second source/drain terminal of the first switching field effect transistor.

In addition, a protective field effect transistor can be provided, the gate terminal of which is coupled to the gate terminal of the first switching field effect transistor, the first source/drain terminal of which is coupled to the second source/drain terminal of the first switching field effect transistor and to a source/drain terminal of a storage field effect transistor, and the second source/drain terminal of which is coupled to a source/drain terminal of another storage field effect transistor.

According to this embodiment, which is implemented in the exemplary embodiment shown in figure 5, a shunt current between storage field effect transistors and switching field effect transistors is avoided, as a result of which the functionality of the circuit arrangement is improved with regard to speed and dynamic power dissipation.

Furthermore, the circuit arrangement can contain a fourth signal path of additional field effect transistors, which has the same circuit as the third signal path formed from the field effect transistors of the flip flop circuit, which additional field effect transistors of the flip flop circuit are

interconnected for storing a complementary storage signal which is complementary to the storage signal.